ABSTRACT OF THE DISCLOSURE

Two first delay signals Q30 and Q34 are generated such that edges thereof are delayed by a first delay time Td1 in relation to the rising edge of a clock signal CLK. Two second delay signals Q32 and Q36 are also generated such that edges thereof are delayed by a second delay time Td2 in relation to the trailing edge of the clock signal CLK. A pulse signal Sout is generated as a result of logic operations performed on the first delay signals Q30 and Q34 and the second delayed signals Q32 and Q36.